DRAM and Storage-Class Memory (SCM) Overview

Introduction/Motivation

Looking forward, volatile and non-volatile memory will play a much greater role in future infrastructure solutions. Figure 1 illustrates a typical processor with its DDR DRAM memory modules (e.g. DIMMs) connected to it. Notice that the integrated memory controller within the processor supports the DDR DRAM bus protocol and only DDR DRAM devices, or those that operate like DDR DRAM, are supported. The tight coupling of computing resources (CPUs, GPUs, FPGAs, etc.) with memory resources pose challenges to memory's expanding importance. These challenges include:

- Memory capacity requirements are increasing, driven by in-memory workloads, server virtualization, etc.
- Compute capacity of CPUs are increasing, requiring more memory controllers and channels per socket
- Fewer high speed DIMMs per channel require more memory controllers and channels to maintain capacity
- Design/support lifecycles for compute and memory resources are tightly coupled making each dependent on the other
- Memory capacity is dependent on the number of CPUs, yielding over-provisioned compute for many workloads

Gen-Z is a new data access technology that can significantly enhance memory solutions built with existing or emerging memory technologies. The following sections are designed to unveil the features and capabilities of the Gen-Z architecture by first describing the foundational features and building on these to illustrate the next generation components and system solutions that are made possible by Gen-Z technology. Note: many components require byte-addressable memory (e.g. CPU, SoC, GPUs, FPGAs, gateways, etc.), but, in this document, the term "processor" will be used to generically describe these roles.

Memory Controller/Media Disaggregation

Figure 2 illustrates an alternate configuration utilizing Gen-Z technology. The core memory controller remains in the processor and initiates high level request (Reads, Writes, etc.), enforces ordering, and performs path selection. The memory media specific logic now resides in a media controller co-located with the memory devices in the external memory modules. A media controller abstracts memory media, translates Gen-Z requests into media specific operations, eliminates tight timing requirements on the processor, and can provide advanced functionality such as transparent caching and acceleration to improve performance. One or more Gen-Z links provide connectivity between the integrated memory controller in the processor and each media controller in the memory modules. A key attribute of Gen-Z memory solutions is that Gen-Z memory can be supported on unmodified operating systems. The detection and initialization of the memory occurs at pre-boot time in system firmware and all memory attributes are reported to the OS via standard software interfaces (e.g. ACPI). Note in Figure 2 that Gen-Z does not necessarily replace direct attached DDR DRAM memory, but can augment it with a variety of memory options. Gen-Z's "disaggregated" architecture enables a range of enhanced features for memory subsystems within a variety of systems.

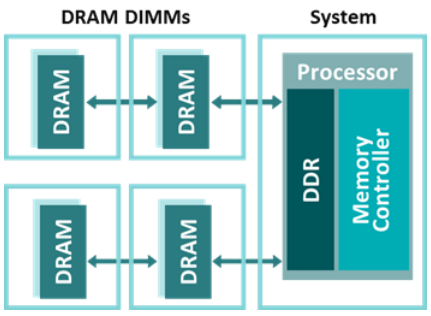

Figure 1: Traditional DRAM

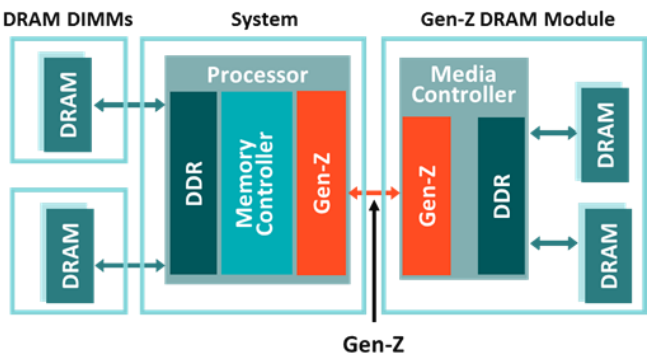

Figure 2: Gen-Z DRAM

Universal Memory Interface

Gen-Z is an abstract device interface that supports a variety of memory types. Besides DDR DRAM memory, there are a number of byte-addressable, persistent, storage class memory technologies that are currently in production, or will be in the near future. Examples are the recently introduced NVDIMM-N (flashed backed DRAM) memory, as well as technologies such as Resistive RAM (Memristor), Phase Change, Spin Transfer Torque, etc. Because requirements for memory subsystems on future platforms may vary widely, Gen-Z provides a universal interface between processors and their memory subsystems, as demonstrated in Figure 3. This architecture yields the following advantages:

- Computing devices and memory technology can evolve independently:
  - Eliminates processor and memory product interlock
  - Accelerates innovation
  - Increases solution flexibility and agility
  - Enables increasing innovation and solution agility
- Computing devices support multiple generations and new types of memory media not anticipated by their original design

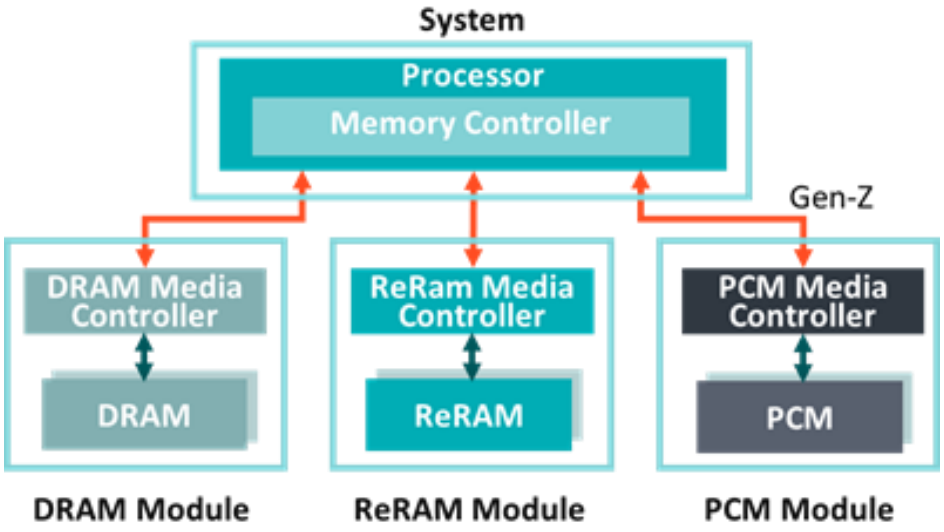

Figure 3: Universal Memory Interface

Flexible, High Bandwidth Serial Interfaces

Gen-Z utilizes high-speed serial physical layer technology supporting 16, 25, 28, 56, and 112 GT/s rates on each serial signal. Gen-Z supports link interfaces that support 1-256 serial signals for transmit and receive (the most common link widths will be 1, 2, 4, 8, or 16 serial signals). Gen-Z interfaces support both copper electrical and optical connectivity between components. Gen-Z supports symmetric link interfaces where there are an equal number of transmit and receive serial signals. Gen-Z also supports asymmetric link interfaces where the number of transmit and receive serial signals is not the same. Asymmetric links enable solutions to tailor read and write bandwidths to application-specific needs, e.g., most applications require higher read bandwidth than write bandwidth.

Figure 4 illustrates single-link read and write bandwidths when operating in symmetric or asymmetric mode. Gen-Z also enables each link to be configured in symmetric or asymmetric link mode at link initialization to enable solutions to adapt to new application needs. This capability demonstrates that component and system providers can “dial in” the proper Gen-Z link configuration to match the bandwidth and capabilities of the native memory media and interconnect behind the Gen-Z media controllers.

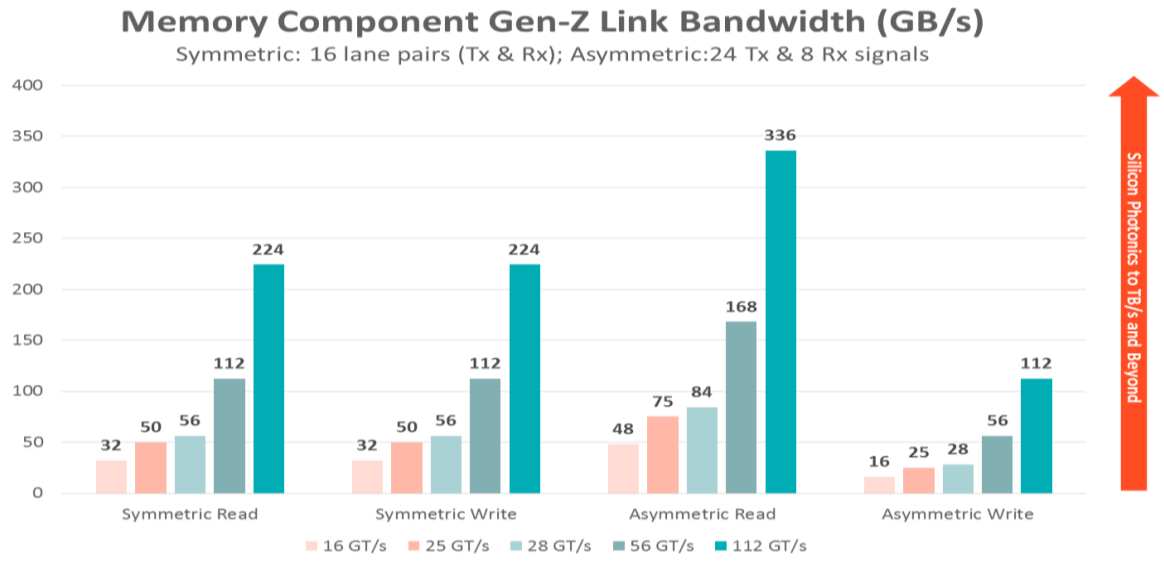

Figure 4: Examples of Gen-Z Memory Component Link Bandwidth

Multipath for Memory

All Gen-Z components can support multiple link interfaces. Multiple links can provide increased aggregate bandwidth, resiliency (eliminates stranded memory), robust and flexible topologies, and supports advanced rich data services. Figure 5 illustrates an example dual-socket server system with a number of Gen-Z memory modules that support DRAM or storage class memory (SCM) media. Memory Module #1 utilizes four symmetric Gen-Z links with 4 lanes per link (for a total of 16 transmit and receive lanes) to connect to processor socket 0. This configuration provides the equivalent bandwidth of a single, wider x16 link, but also provides a new capability not found in today's memory subsystems: resiliency in the event of link and path failures. For example, if link A failed, then processor 0 and Memory Module #1 will continue to use links B-D for operations. A key aspect of Gen-Z's resiliency features include link level and end-to-end retries and timers such that during link and path failures, the low level Gen-Z logic automatically recovers operations without impacting upper layer component functionality. This provides a consistent resiliency feature across all component types and vendors.

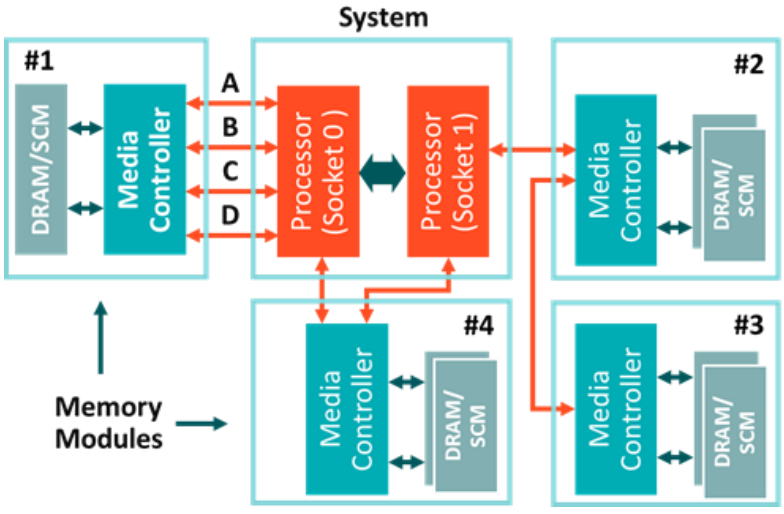

Figure 5: Gen-Z Enables Memory Subsystem Design Flexibility

Gen-Z's multipath, multi-link feature also enables flexible topologies for memory subsystems in a platform. Figure 5 provides several examples of topology alternatives supported by Gen-Z. Memory Modules #2 and #3 are connected in a daisy chain

configuration. Processor 1 is connected with a single Gen-Z link to Module #2 and Module #3 is daisy-chained to Module #2 with another single Gen-Z link, thus providing high capacity without utilizing additional processor Gen-Z links. Another topology supported by Gen-Z is that used by Memory Module #4. Here, the module supports two Gen-Z links (of any width), with one link connected to Processor 0 and the other connected to Processor 1. This topology facilitates a memory subsystem on a dual-socket server where memory access does not have to transit the interprocessor link (IPL) between the processors. This improves memory performance and frees the IPL for other low-latency coherency operations between the processors.

Fabric Attached Memory (FAM)

Gen-Z not only enables point-to-point topologies, but also facilitates the concept of fabric attached memory when systems employ Gen-Z switches. Figure 6 illustrates an example configuration where fabric attached memory can enable enhanced platform and infrastructure capabilities to support existing and next generation workloads. Figure 6 depicts a single socket server that uses a standalone Gen-Z switch to expand the number of memory modules. This configuration enables capacity expansion beyond the number of Gen-Z links provided in the processor itself, and enables any system to support any scale of in-memory application.

Figure 7 illustrates a rack scale configuration with multiple servers/processors are connected to each other and with multiple memory modules through a Gen-Z switch. This configuration can enable a variety of memory sharing schemes including:

- Memory module leasing – entire module is “owned” by one processor at a time; ownership can change as workloads require
- Memory region leasing – memory regions within memory modules are “owned” by one processor at a time, and ownership can change as workloads require. Multiple processors can utilize the memory in a module at the same time (but not the same regions at the same time)
- Full memory region sharing – memory regions within the memory modules can be allocated to more than one processor at the same time to facilitate collaborative workloads in scale-out deployments

In all of the above cases, software-defined management provides memory resource provisioning services. Gen-Z enables enhanced memory-centric computing where data can be directly sourced and manipulated in fabric attached memory by threads of execution running on one or more compute devices (processors, FPGAs, GPUs, etc.) simultaneously. This significantly reduces data movement to improve performance, reduce power consumption, reduce capital and operational costs, etc. Fabric-attached memory helps break the hard linkage between compute resources and memory resources. Today, the amount of memory present in the infrastructure depends on the number of processors or other processors that are present. Fabric attached memory allows memory resources to be added, provisioned, and removed independently of computing resources in the same infrastructure. Thus, Gen-Z enables infrastructure operators to have more flexibility to define the composition of their infrastructure to suit the needs of the workloads that must be delivered to their customers.

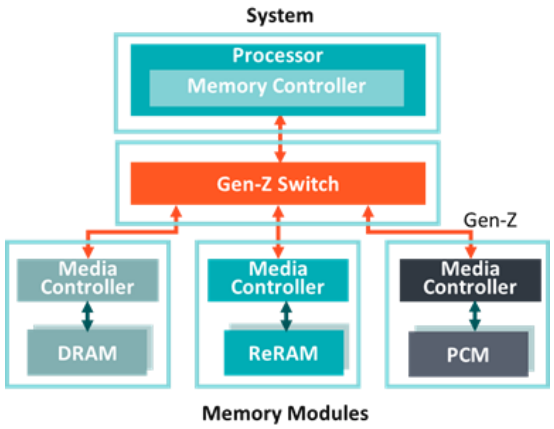

Figure 6: Local Memory Expansion

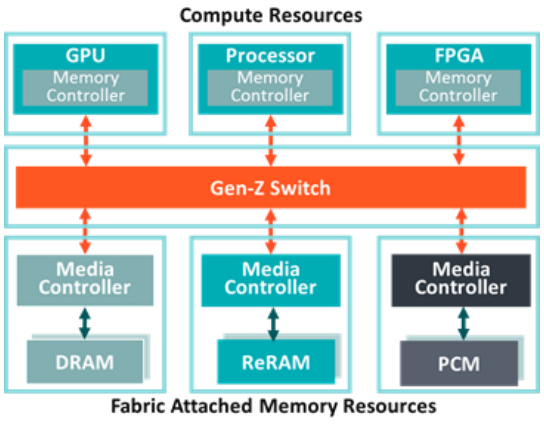

Figure 7: Fabric Attached Memory

Enhanced Mechanical Packaging and Deployment Options

Figures 8 and 9 depict system concepts that can be used to implement the logical topologies shown in Figures 3 and 6. Figure 8 demonstrates using Gen-Z to facilitate flexible system designs. This figure depicts a standard dual-socket server motherboard that utilizes both standard DRAM DIMM memory modules and Gen-Z memory modules. Due to strict signal routing and length requirements, the DIMM modules must be placed close to the processors. Gen-Z does not impose such constraints, which allows Gen-Z modules to be placed in locations that optimize the server's configuration, power, and cooling infrastructure.

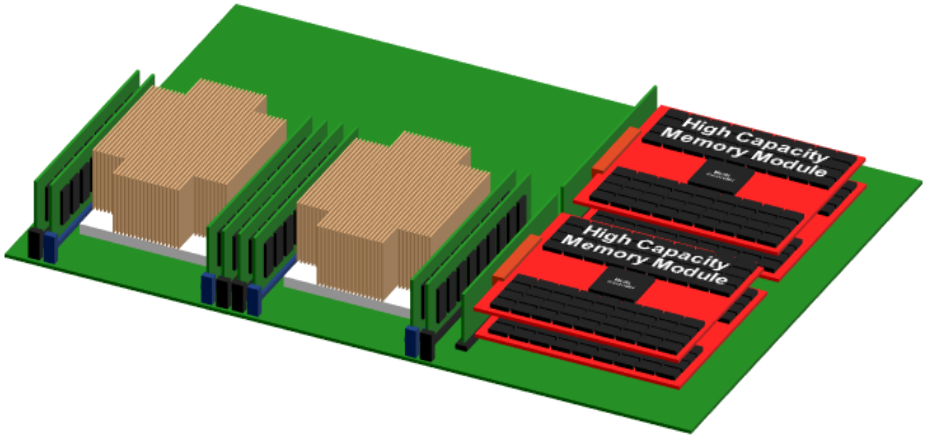

Figure 8: Gen-Z Enables Flexibility in Internal Memory Subsystem Placement

Figure 9 depicts an alternative memory subsystem form factor that utilizes external, serviceable memory modules similar to storage drives. Gen-Z enables memory solutions that can utilize existing form factors, e.g. 2.5" or 3.5" disk drive form factors, or new memory optimized form factors to support serviceable storage class memory subsystems. Thus, Gen-Z enables memory solutions with thermal characteristics and mechanical form factors optimized for a wide variety of system design requirements.

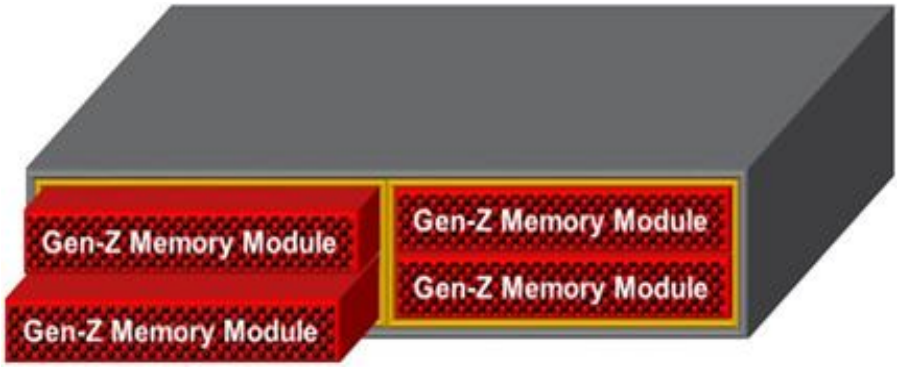

Figure 9: Gen-Z Enables Flexibility in External Memory Subsystem Placement

Figure 10 demonstrates an example rack-scale implementation using Gen-Z enabled compute and memory components. This figure depicts a rack with a relatively large number of bays that can accommodate a variety of Gen-Z enabled components. The bays are filled with any combination of compute (CPUs, GPUs, FPGAs, etc.) and fabric attached DRAM Memory or Storage Class Memory (SCM) modules. Like compute modules today, different sizes or capacities of memory modules can be accommodated by using larger modules that fill multiple adjacent bays. Gen-Z switches tie these and other types of Gen-Z enabled component modules together to create a composable infrastructure where memory is now a peer resource with compute, storage and networking.

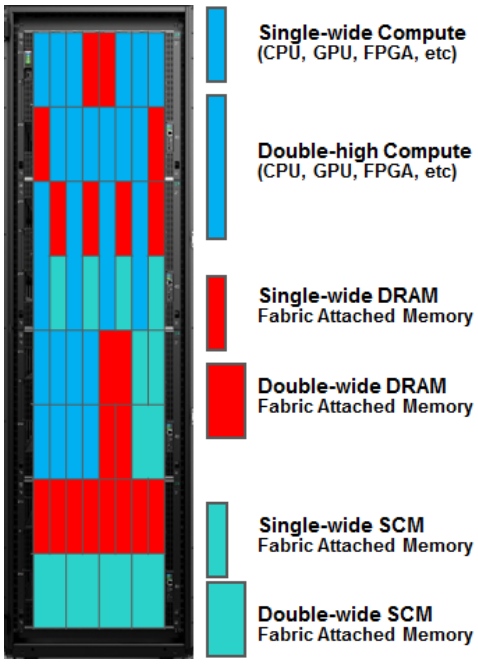

Figure 10: Example: Rack-scale Fabric Attached Memory Deployment

Security

Memory semantic technology like Gen-Z, where memory resources are mapped for a wide variety of components to have access presents security challenges. This is particularly true in the case of fabric attached memory where memory resources can possibly be accessed from any compute or other component types in the fabric. The Gen-Z architecture supports a combination of hardware-enforced isolation techniques and full packet authentication to prevent errant or malicious components from communicating with unauthorized components or accessing unauthorized resources, including memory.

Summary

Gen-Z technology is designed to supplement platforms and infrastructure with capabilities for a new generation of byte addressable memory solutions that will be difficult or impossible to achieve with existing memory, memory interfaces, and interconnect technology. These capabilities include:

- A “disaggregated” memory architecture that facilities a universal memory interface
  - Allows CPUs, GPUs, FPGAs, and other host components to evolve independent of memory
  - Supports multiple memory media types, include DRAM and Storage Class Memory technologies
  - Can be supported with unmodified operating systems
- Offers a robust roadmap of standard serial interface technology for electrical and optical interconnect
  - Selectable link widths, speeds, and modes enables bandwidth for today and well into the future
  - Enables enhanced memory subsystem form factors and system packaging options
- Gen-Z offers the first full featured, general purpose multipath solution for memory subsystems
  - Provides bandwidth, link and path failure resiliency, and flexible topology options
- Gen-Z was developed to be the platform for fabric attached memory
  - Gen-Z scales from point-to-point, to local memory expansion through switches, to rack-scale solutions
- Gen-Z offers security features that protect and isolate an infrastructure’s valuable memory assets

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