Gen-Z ZMMU and Memory Interleave

April 2019
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ZMMU

- Gen-Z supports two MMU (Memory Management Unit) types:
  - Requester ZMMU
    - Used to map Responder addressable resources
    - Enables application-transparent access, e.g., processor load-store operations are transparently translated to Gen-Z read and write operations that target a specific memory component
    - Applicable only to explicit OpClass operations
      - Gen-Z assumes memory-controller integration to optimize load-to-use latency for P2P-Core OpClass memory. Hence, P2P-Core relies exclusively upon Requester-specific decoding and interleaving
  - Responder ZMMU
    - Used to translate the packet’s Address into Responder-specific media device addresses
    - Used to enforce page-level access permission (R-Keys)
  - Components that act as both a Requester and as a Responder can support both ZMMU types
    - For example, processors, I/O components, memory / storage modules that support third-party data moves, etc.
    - Much of the underlying ZMMU IP can be re-used to implement Requester and Responder ZMMUs
  - Gen-Z specifies two ZMMU designs:
    - Page Table-based ZMMU
    - Page Grid-based ZMMU
Example Component with Requester ZMMU
Example Component with Responder ZMMU

- Request Packet
- (OpCode, Gen-Z Address, ...)
- Address Decode Logic
- Component A
  - Gen-Z Responder Memory Management Unit
    - Page Table Entry Address A'
    - Page Table Entry Address B'
    - Page Table Entry Address X'
    - Page Table Entry Address C'
    - Page Table Entry Address L'
    - Page Table Entry Address Y'
    - Page Table Entry Address K'
    - Page Table Entry Address Z'
  - Responder-Local Addressable Resources
    - Page X
    - Page Y
    - Page Z
Page Table-based ZMMU Structure
Page Table Pointer-Pair ZMMU Table Entry

- This table entry is used to locate either another level of tables or a table of PTE entries
  - ET indicates if the table entry is valid
  - PT0 and PT1 indicate if the pointer is valid and to what is points
A Page Grid is a highly-efficient alternative to a Page Table-based ZMMU that uses on-die resources instead of a hardware page table walker and caching resources to provide optimal performance.
### Requester PTE

<table>
<thead>
<tr>
<th>PASID</th>
<th>TC</th>
<th>Write Mode</th>
<th>NSE</th>
<th>LPE</th>
<th>PEC</th>
<th>PME</th>
<th>PSE</th>
<th>WPE</th>
<th>SKE</th>
<th>CE</th>
<th>CCE</th>
<th>DRC</th>
<th>ST</th>
<th>D-ATTR</th>
<th>ET</th>
<th>V</th>
<th>&lt; LSB</th>
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<td>R-Key</td>
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<td>TR Index</td>
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<td>ADDR [63:12]</td>
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### Data Space Requester PTE

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<td>R-Key</td>
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<td>TR Index</td>
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## Responder PTE

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**MSB >**
Memory Interleaving

- Memory interleaving is used to improve aggregate bandwidth and latency by distributing memory across multiple components.
  - In this example, memory is distributed across four Responders providing up to 4x improvement in aggregate bandwidth

- Memory interleaving can be enhanced using RAID, erasure codes, etc. to distribute resiliency information across multiple Responders to improve data availability

- Gen-Z specifies a barber pole interleave scheme that supports up to 64-way interleaves
Example 3-way Stack Barber Pole Memory Interleave

Interleave Range 2
1.5 TiB

Interleave Range 1
1.5 TiB

Interleave Range 0
1.5 TiB

Output Address from Requester’s ZMMU

Responder CID 0
Sparse Address Space Delimited by DCID (3-way Interleave)

Responder CID 1

Responder CID 2

Packed Media Address Space Post Responder Masking Off High-Address Bits

Interleave Range 2
1.5 TiB

Interleave Range 1
1.5 TiB

Interleave Range 0
1.5 TiB

Output Address from Requester’s ZMMU

Responder CID 0
Sparse Address Space Delimited by DCID (3-way Interleave)

Responder CID 1

Responder CID 2

Packed Media Address Space Post Responder Masking Off High-Address Bits
A component such as a SoC may impose component-specific requirements and constraints on interleaves. For example, interleave between SoC home agents, vendor-specific coherency links, cache line slices, etc.
Vendor-specific P2P-Core Memory Interleave

Example SoC #1

- CPU Cores
- Vendor-specific address decode / Interleave
- Vendor coherence Fabric or NoC
- Home Agent 1
- Requester PE
- Responder 1
- Responder 2

Requests steered to one of four home Agents – two per SoC

Vendor-specific Coherency

Example SoC #2

- CPU Cores
- Vendor-specific address decode / Interleave
- Vendor coherence Fabric or NoC
- Home Agent 1
- Requester PE
- Responder 3
- Responder 4
- Home Agent 2
- Requester PE
Transparent Memory Interleave

TR Requester(s) see TR as a High-Capacity Memory Component

Requester

Responder 1
Responder 2
Responder 3
Responder 4

TR Translation and Interleave Logic
Switch
Thank you